Reference material

Aspect Controls and Indications in CBI Systems with Relay Interface

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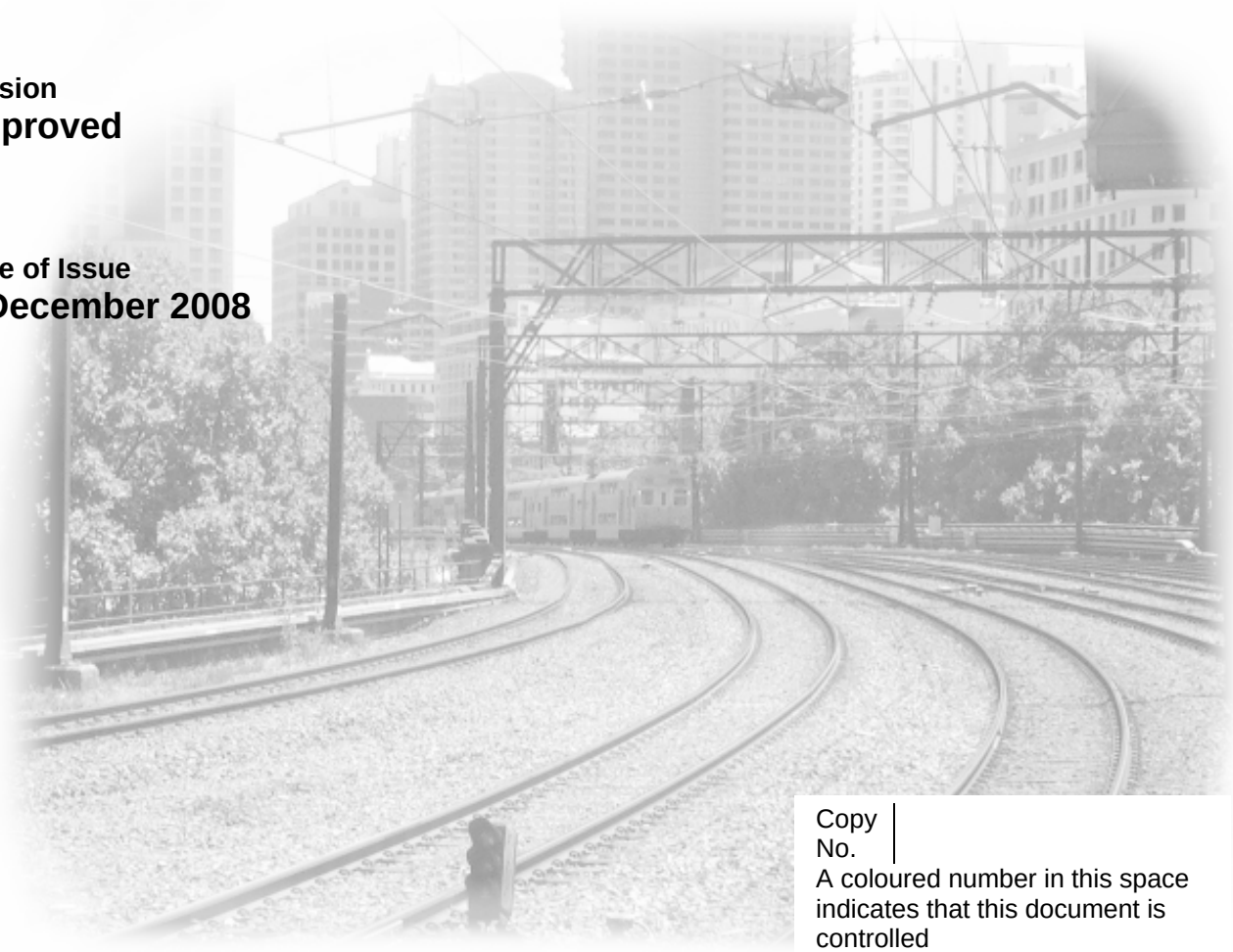
Aspect Controls and Indications in CBI Systems with Relay Interface

Design Guideline

Version
Approved

Date of Issue
1 December 2008



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Design Guideline

Version
Approved

1 December 2008

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1 BACKGROUND

The use of distributed CBI systems operating relay interfaces results in the need to prove that a signal is actually displaying a specific aspect before signals in advance can also step up their aspect.

This document discusses the degree to which both internal aspect bits and external aspect proving are combined in the system data.

These concepts are not applicable to a system where signal lamps are directly driven.

This document also addresses data arrangements that promote consistency in the receipt of signal status information by the control system and thus the signaller.

2 SYSTEM CONFIGURATION

The type of system where this issue arises is where a central interlocking performs all data statements, and distributed slaves pass signal aspect relay controls directly to output relays.

These relays are then proved back into the system.

The proved input is fed back to the interlocking for aspect control on other signals.

None or only minor processing is performed in the slave.

The system configurations and the data flows are shown in Appendix A.

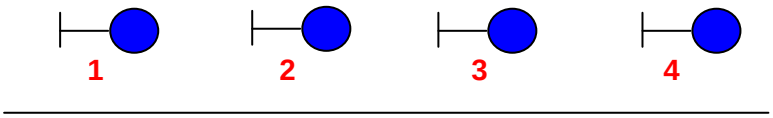
3 SYSTEM ISSUES

When a signal is cleared to show a proceed indication or steps to a higher indication, proving of that indication is required before the signal in the rear's aspect output can be driven to it's next higher indication.

This is obtained by proving the aspect control up, back into the slave and through to the interlocking.

The aspect control of the signal in the rear, could be constructed using only the aspect proving functions.

For example:



Basic Logic:

3HR * 2HR = 2HDR

Definitions: A 'P' indicates a proving input from the field

An 'R' indicates a purely internal function

Note: It is considered that the HR (slave output) includes proving of the train stop reverse, hence VRR function does not need to be separately included.

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In order to prove the external function, the above logic would be:

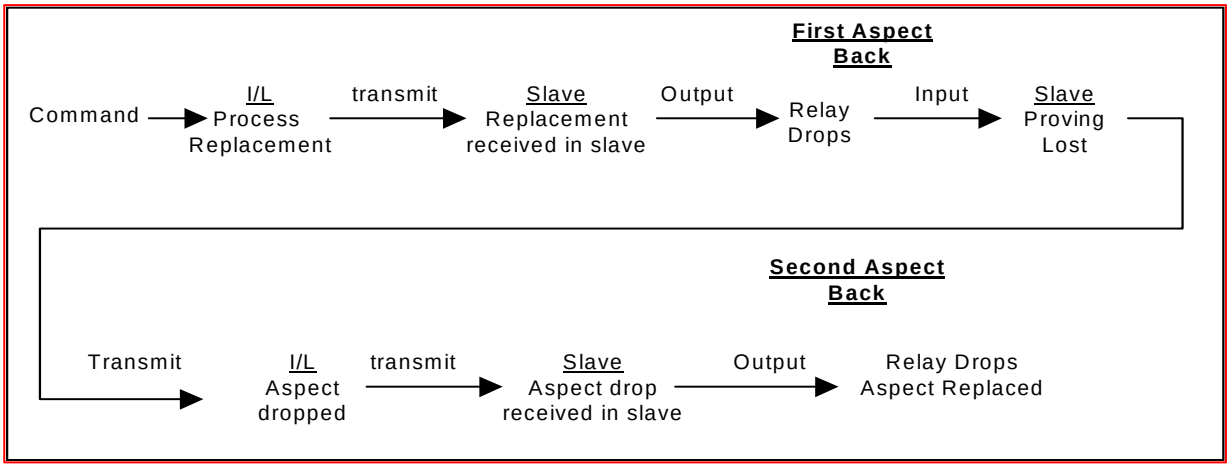
3HP * 2HR = 2HDR

If signal 3 is replaced, signal 2 will be dependent on the loss of the HP bit before 2HDR is lost.

A hazard may exist with the timing between the replacement of 3 and the loss of 2 HDR. This is because the replacement of 3 in the interlocking has to propagate through to the slave and drop the output relay. The consequent loss of the proving input then propagates back to the interlocking to replace the aspect equation which then, again propagates to the slave to replace the higher aspect.

This is likely to take 2-3 seconds.

SEQUENCE OF EVENTS

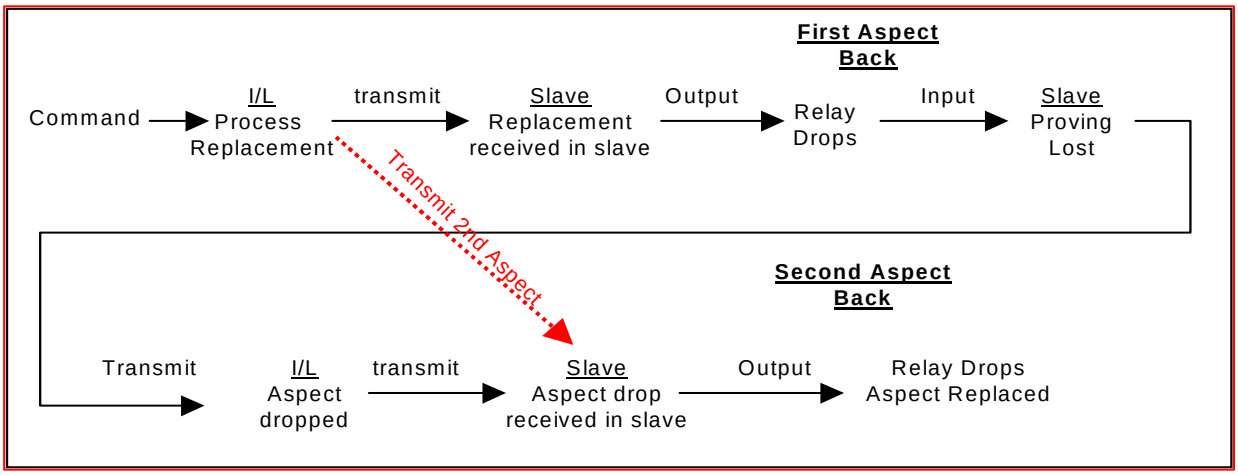


During this period an irregular aspect sequence may be observed if all signals were able to be seen together. However, the situation is safe as in the scenario of an aspect replacement, approach locking would hold the interlocking and is designed to specifically cover this situation.

To prevent the momentary display of an irregular aspect sequence, the aspect sequence can be replaced in the interlocking directly. This requires the internal aspect function to be also provided in the aspect equation.

3HR * 3HP * 2HR = 2HDR

In this arrangement the sequence of events is as follows:



This diagram shows that the two aspects will now restore simultaneously.

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4 SLAVE AND MASTER DATA

4.1 Slave Data

The basic caution output contains the trainstop detection.

2AT (input) * **2VRR** (input) * **2HR** (from master) = **2HR** (output)

Within the slave the corresponding logic to drive the output for higher aspect is

2HDR (from master) * **2HR** (from master) * **2HP** = **2HDR** (output)

↑ signaller replaces ↑ local track replaces

4.2 Master Data

The corresponding master data:

3HR * 3HP * 2HR = 2HDR (to send to slave)

5 ARRANGEMENT OF SIGNAL REPEATERS

In relay based interlocking systems, it is usual practice to drop the NGP & consequently the NGK relays when the route control relay (UCR) picks. This is to permit the vital down proving of the relay. Adopting this approach in a CBI system will result in a delay between the loss of the red repeater, and obtaining the green repeater by the time taken for the control to reach the output relay and return via the serial links and field equipment.

It is possible to reduce this delay by ensuring the signal repeater more closely represents the actual state of the field equipment.

Accordingly, the bit sent to the control system shall be a separate NGK bit derived from the field NGP bit, but without the ~UCR function in the interlocking.

NGPZ * VNR = NGK

As a consequence of this the NGK will be up with the ALSR down during the signal clearing process. This would result in the display of a flashing red during signal clearing, which is undesirable. Accordingly, the ALSK indication to the control system needs to be amended as follows:

(ALSR + UCR) * NGK = ALSK

This expression will result in no change to the current control system logic.

The reverse repeater logic remains as:

HP * VRR = RGK

The outcome is that the red to green transition of the signal repeater will reflect the trainstop operation time closely, and transmission delays being common to both normal and reverse indications will be transparent to the operator.

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6 BI-DIRECTIONAL SYSTEM WITH TRAIN STOPS

When two-way operation is provided, the train stop may be operated by two controls:

- When the signal associated with the train stop clears
- When the trainstop needs to be suppressed for an opposing direction movement.

It is usual for the trainstop to be driven by the interlocking HR output being received by the slave. Upon receipt of the VRR, the signal HR output is energised thus clearing the signal.

The typical equation is shown at 4.1.

With a bi-directional system, the trainstop may also need to be suppressed by opposing signals and proved reverse in the higher aspects of those signals. To achieve this, a train stop suppression bit is sent from the interlocking to the slave to also drive the trainstop.

(2HR * 2AT) + 2VSN = 2VR

The VSN bit is also used to qualify the NGK equation:

2NGPZ * (2VNR + 2VSN) = 2NGK

7 CONCLUSION

While all external proving aspects are to be included for step up purposes, the internal bit also needs to be included for stepping down aspects. Data needs to consider the actual result required in order to avoid undue timing delays. The indications should reflect the state of the function and not be unduly affected by the operation (or proving) of other functions that may mask any situation that could be a less desirable outcome.

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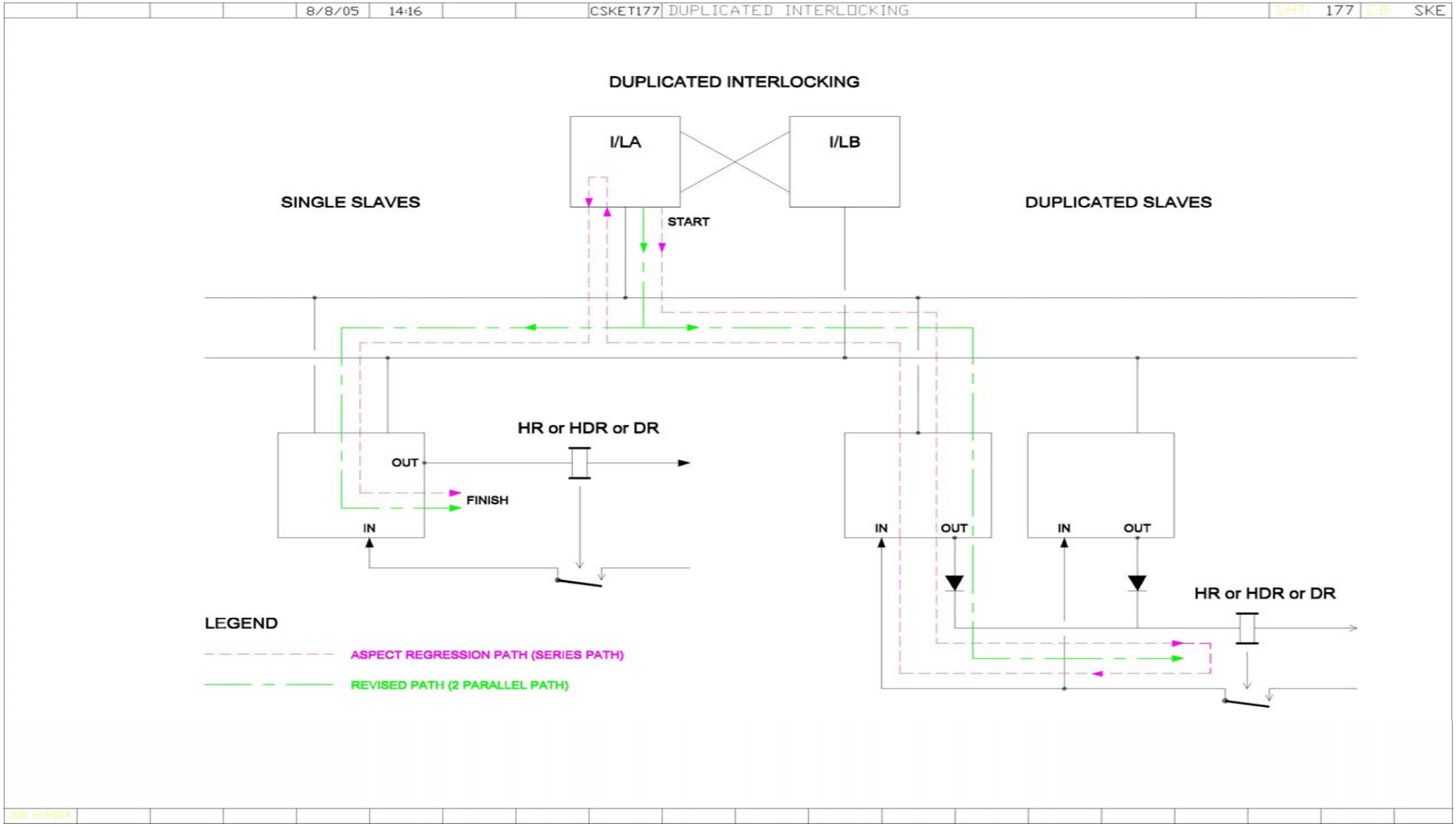
8 APPENDIX A – TYPICAL SYSTEM CONFIGURATION AND DATA FLOW



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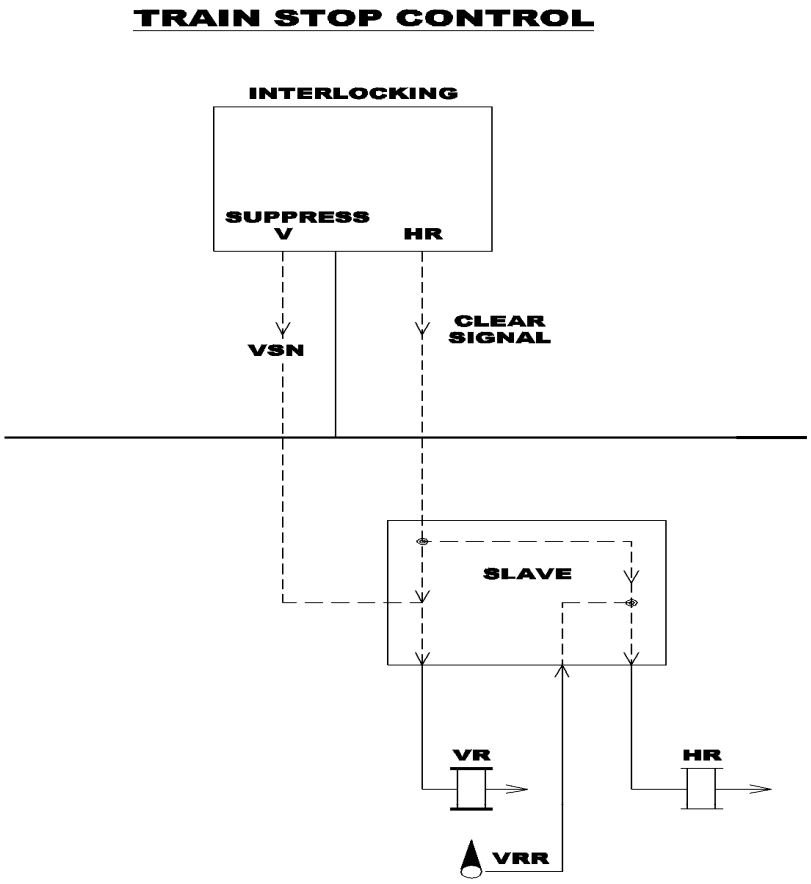
9 APPENDIX B – TRAIN STOP CONTROL



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